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SF-6489

B. E. - II (Sem. IV) (EC / ECC) Examination

May / June - 2011

Digital Circuits

Time : **3** Hours] [Total Marks : **100**

Instructions :

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :

☛ B. E. - 2 (SEM. 4) (EC / ECC)

Name of the Subject :

☛ DIGITAL CIRCUITS

☛ Subject Code No. : 6 4 8 9 ☛ Section No. (1, 2,.....) : NIL

Seat No. :

Student's Signature

(2) Attempt all questions.

(3) Assume suitable data whenever required.

(4) Use of scientific calculator (82-fx, 82Ms, 100-fx and 100-Ms or equivalent) of other companies is allowed.

1 (a) Attempt following : **5**

(i) Which of the binary number is equivalent to decimal 10

(a) 1000 (b) 1100

(c) 1010 (d) 1001

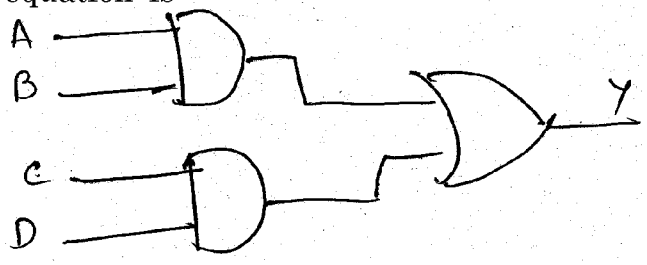
(ii) $(101101)_2 - (100111)_2 =$ _____

(iii) The parity bit is

(a) always 1 (b) always 0

(c) 1 or 0 (d) none of above

(iv) For the circuit shown in figure 1 the output equation is



(a) $Y = ABCD$ (b) $Y = AB + \overline{CD}$

(c) $Y = A+BCD$ (d) $Y = AB + \overline{CD}$

(v) $\overline{A} \cdot \overline{B} \cdot \overline{C}=F$ represents a

(a) NOR gate (b) NAND gate

(c) Ex-OR gate (d) AND gate

(b) Represent the decimal number 8620 **4**

(i) In BCD

(ii) In Excess-3 code

(iii) In 2421 code

(iv) As binary No

(c) Design and implement a 4-bit binary to gray converter. **6**

(d) Explain the function of NAND gate and explain that why it is called universal gate. **5**

2 Attempt any two : **16**

(a) Express the following functions in a sum of minterms and a product of max terms

(i) F (A, B, C, D) = D (A' + B) + B'D

(ii) F (x,y,z) = 1

(b) Simplify the following Boolean function using K-map

(i) f (w,x,y,z) = $\sum$ (0,1,2,4,5,6,8,9,12,13,14)

(ii) f = A'B'C' + B'CD' + A'BCD' + AB'C'

(c) Design an SOP circuit that will generate an odd parity bit for a 4-bit input.

3 Attempt any two : **14**

(a) Write short note on magnitude comparator and draw the ckt for the same.

(b) Explain look ahead carry generator in detail.

(c) Design full subtractor using half subtractor and gate.

(d) Explain and draw the circuit for BCD adder using binary parallel adder IC.

4 (a) Answer the following questions (each of 1 mark) **10**

(i) If J=K=1 in JK flip flop, what will be the next state output Q (t+1) if the previous state output was Q (t)=1 ?

(ii) Define Sequential circuits.

(iii) What is the advantage of state reduction method ?

(iv) State true or false : "A Serial in Parallel out (SIPO) register can have all of its bits displayed at one time."

(v) State atleast two application of MUX.

(vi) How many flip flops are required to construct mod-15 counter.

(vii) Give the definition of Encoder.

(viii) What is the difference between bidirectional shift register and unidirectional shift register ?

(ix) How many flip flops are required to construct 5 bit shift register ?

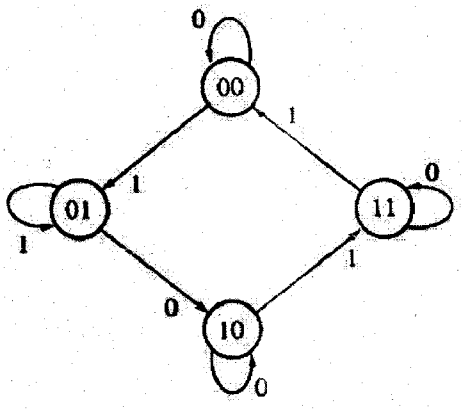
(x) A single flip flop may be used to divide the input frequency by_____.

(b) Implement a full adder circuit with a decoder and two OR gates. **5**

(c) Explain in detail 4 to 1 line multiplexer. **5**

5 (a) Explain in detail Master Slave flip flop. **7**

(b) Design a sequential circuit for the state diagram shown below. **8**



OR

5	(a)	Explain in detail clocked Rs flip flop.	**7**
	(b)	Convert T flip flop into D flip flop.	8
6	(a)	Explain bidirectional shift register with parallel load.	**7**
	(b)	Design 3 bit binary up ripple counter using JK flip flop.	8

OR

6	(a)	Explain Johnson counter in detail.	**7**
	(b)	Draw and explain 4 bit shift register with parallel load.	8